IN THE CLAIMS

Claim 1 (Currently Amended): A method for fabricating a semiconductor device, comprising the steps of:

a) forming a stack layer of a gate layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate;

b) carrying out a selective oxidation process adopting a rapid thermal process (RTP), wherein the poly-silicon layer of the stack layer is only oxidized;

c) performing a heat treatment process in a vacuum ambient of a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress caused by the RTP; and

d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer.

Claim 2 (Previously Presented): The method as recited in claim 1, wherein the heat treatment process and the gate sealing nitride layer formation process are carried out by using the LPCVD furnace under an in-situ method.

Claim 3 (Currently Amended): The method as recited in claim 2, wherein the in-situ method includes the steps of:

a1) loading the semiconductor substrate at which the selective oxidation process is carried out in the LPCVD furnace;

b1) carrying out the heat treatment process by slowly increasing a temperature of the LPCVD furnace from a room temperature to a target temperature for the heat treatment process and keeping the target temperature in ~~a~~ the vacuum ambient;

c1) depositing the gate sealing nitride layer after slowly decreasing the temperature of the LPCVD furnace from the target temperature for the heat treatment process to a target temperature for depositing the gate sealing nitride layer; and

d1) unloading the semiconductor substrate after decreasing the temperature of the LPCVD furnace to a room temperature.

Claim 4 (Original): The method as recited in claim 3, wherein the target temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

Claim 5 (Original): The method as recited in claim 3, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

Claim 6 (Original): The method as recited in claim 3, wherein a falling rate of the temperature for depositing the gate sealing nitride layer ranges from about 1 °C/min to about 20 °C/min.

Claim 7 (Original): The method as recited in claim 3, wherein the heat treatment process is carried out for about 10 minutes to about 240 minutes.

Claim 8 (Previously Presented): The method as recited in claim 1, wherein the heat treatment process and the gate sealing nitride layer formation process carried out in the same LPCVD furnace or two different LPCVD furnaces under an ex-situ method.

Claim 9 (Previously Presented): The method as recited in claim 8, wherein the ex-situ method includes the steps of:

a2) loading the semiconductor substrate at which the selective oxidation process is carried out in a first LPCVD furnace;

b2) performing the heat treatment process by slowly increasing a temperature of the first LPCVD furnace from a room temperature to a target temperature for the heat treatment process and keeping the target temperature in a vacuum ambient;

c2) unloading the semiconductor substrate after decreasing the temperature of the LPCVD furnace to a room temperature; and

d2) depositing the gate sealing nitride layer after loading the unloaded

semiconductor substrate in the first LPCVD furnace or a second LPCVD furnace.

Claim 10 (Original): The method as recited in claim 9, wherein the target temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

Claim 11 (Original): The method as recited in claim 9, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

Claim 12 (Original): The method as recited in claim 9, wherein a falling rate of the temperature for depositing the gate sealing nitride layer ranges from about 1 °C/min to about 20 °C /min.

Claim 13 (Original): The method as recited in claim 9, wherein the heat treatment process is carried out for about 10 minutes to about 240 minutes.

Claim 14 (Currently Amended): A method for fabricating a semiconductor device, comprising the steps of:

a3) forming a stack layer of a gate oxide layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate;

b3) carrying out a selective oxidation process, wherein the poly-silicon layer of the stack layer is only oxidized;

c3) depositing a gate sealing nitride layer on the stack layer selectively oxidized by low pressure chemical vapor deposition (LPCVD);

d3) performing a heat treatment process in a vacuum or inert gas ambient of an LPCVD furnace or an annealing furnace for releasing a stress exerted during the selective oxidation process and gate sealing nitride layer deposition process; and

e) performing a rapid thermal process (RTP) for activating source/drain regions of the semiconductor device.

Claim 15 (Previously Presented): The method as recited in claim 14, wherein the gate sealing nitride layer deposition process and the heat treatment process are carried out in the identical furnace or in two different LPCVD furnaces under an ex-situ method.

Claim 16 (Currently Amended): The method as recited in claim 15, wherein the ex-situ method includes the steps of:

a4) depositing the gate sealing nitride layer on the semiconductor substrate in a first LPCVD furnace;

b4) loading the semiconductor substrate on which the gate sealing nitride layer is deposited in a second LPCVD furnace;

c4) performing the heat treatment process by slowly increasing a temperature of the second LPCVD furnace from a room temperature to a target temperature for the heat treatment process and maintaining the target temperature in ~~a~~ the vacuum or inert gas ambient; and

c5) unloading the semiconductor substrate after decreasing the temperature of the second LPCVD furnace from the target temperature for the heat treatment to a room temperature.

Claim 17 (Original): The method as recited in claim 15, wherein the ex-situ method includes the steps of:

a6) depositing the gate sealing nitride layer in the LPCVD furnace;

b6) loading the semiconductor substrate on which the gate sealing nitride layer is deposited in an annealing furnace used for the heat treatment process;

c6) carrying out the heat treatment process by increasing a temperature of the annealing furnace from a room temperature to a target temperature for the heat treatment process and maintaining the target temperature in a vacuum or inert gas ambient; and

d6) unloading the semiconductor substrate after decreasing the temperature of the annealing furnace.

Claim 18 (Original): The method as recited in claim 16, wherein the temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

Claim 19 (Original): The method as recited in claim 16, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

Claim 20 (Original): The method as recited in claim 16, wherein a falling rate of the temperature for the heat treatment process ranges from about 1 °C /min to about 20 °C /min.

Claim 21 (Original): The method as recited in claim 17, wherein the temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

Claim 22 (Original): The method as recited in claim 17, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

Claim 23 (Original): The method as recited in claim 16, wherein a falling rate of the temperature for the heat treatment process ranges from about 1 °C /min to about 20 °C /min.